CLAIMS

We claim:

1. A trench DMOS transistor cell comprising:

a substrate of semiconductor material of heavily doped first electrical conductivity type;

a first covering layer of semiconductor material of first conductivity type lying on the substrate;

a second covering layer of semiconductor material of second electrical conductivity type lying on the first covering layer and having a bottom surface;

a third covering layer of semiconductor material of heavily doped first conductivity type and having a top surface and partly lying over the second covering layer, where a portion of the second covering layer is heavily doped and this portion extends vertically upward through a portion of the third covering layer to the top surface thereof;

a trench having a bottom surface and side surfaces and extending vertically downward from the top surface of the third covering layer through the third and second covering layers and through a portion of the first covering layer, where the bottom surface of the trench lies above a lowest part of the bottom surface of the second covering layer;

electrically conducting semiconductor material positioned within the trench;

a layer of oxide positioned within the trench between the electrically conducting semiconductor material and the bottom and side surfaces of the trench; and

three electrodes electrically coupled to the electrically conducting material, to the third covering layer and to the substrate, respectively.

2. A trench DMOS transistor cell comprising:

a substrate of semiconductor material of heavily

doped first electrical conductivity type having a top surface;

a first covering layer of semiconductor material of first conductivity type having a top surface and being contiguous to and overlying the substrate top surface;

a second covering layer of semiconductor material of second electrical conductivity type having a top surface and being contiguous to the top surface of the first covering layer and extending vertically downward from the top surface of the first covering layer into an upper portion of the first covering layer;

a third covering layer of semiconductor material of heavily doped first conductivity type having a top surface and being contiguous to and partly overlying the top surface of the second covering layer, where a portion of the second covering layer is heavily doped and this portion extends vertically upward through the third covering layer to the top surface thereof and forms an exposed pattern of the second covering layer adjacent in the top surface of the third covering layer, where the maximum depth of the heavily doped portion of the second covering layer relative to the top surface of the third covering layer is a predetermined number d_1, and where the depth of the top surface of the substrate at a position that underlies the position of maximum depth of the heavily doped portion of the second covering layer is a second predetermined number d_2;

a trench having side surfaces and bottom surfaces and extending vertically downward from the top surface of the third covering layer through the third covering layer, through the second covering layer and through a portion of, but not all of, the first covering layer, the trench bottom surface having a maximum depth relative to the top surface of the third covering layer equal to a third predetermined number d_3 where $d_3 < d_1$, where the trench in horizontal cross section is

approximately a polygonal stripe with stripe width approximately equal to a fourth predetermined number b, and where this polygonal stripe laterally surrounds and is spaced apart from the exposed pattern of the second covering layer at the top surface of the third covering layer;

a layer of oxide, positioned within the trench and contiguous to the bottom surfaces and side surfaces of the trench so that a portion of, but not all of, the trench is filled with this oxide layer;

electrically conducting semiconductor material, having resistivity of approximately one ohm-cm, that is contiguous to the oxide layer and positioned within the trench so that this electrically conducting material is spaced apart from the side walls and the bottom walls of the trench by the oxide layer; and

three electrodes that are electrically coupled to the electrically conducting semiconductor material in the trench, to the third covering layer and to the substrate, respectively.

3. A cell according to Claim 2, wherein said substrate has a doping concentration of at least $10^{18}cm^{-3}$.

4. A cell according to Claim 2, wherein said first covering layer has a doping concentration in the range of 10^{15}-$10^{17}cm^{-3}$.

5. A cell according to Claim 2, wherein said vertically extending portion of said second covering layer has a doping concentration of at least $10^{18}cm^{-3}$.

6. A cell according to Claim 2, wherein said third covering layer has a doping concentration at the top surface of at least $5x10^{19}cm^{-3}$.

7. A cell according to Claim 2, wherein the shape of said polygonal stripe is drawn from the class consisting of

a hexagon, a circle and an oval.

8. A cell according to Claim 2, wherein said second covering layer exposed pattern has the shape of a hexagon.

9. A cell according to Claim 2, further comprising a second oxide layer contiguous to said electrically conducting trench material within said trench.

10. A cell according to Claim 7, further comprising a trench-filling semiconductor material that is contiguous to said second oxide layer within said trench and that substantially fills the remainder of said trench.

11. A cell according to Claim 2, wherein the difference d_1-d_3 between said predetermined numbers d_1 and d_3 is 0.5μm or greater.

12. A cell according to Claim 2, wherein the difference d_2-d_1 between said predetermined numbers d_2 and d_1 is 1.25 μm or less.

13. A cell according to Claim 2, wherein said trench oxide layer has a thickness on said side surfaces and said bottom surfaces of said trench that lies in the range 0.1-0.2 μm.

14. A method for providing a trench DMOS transistor cell, the method comprising the steps of:

providing a substrate of semiconductor material of heavily doped first electrical conductivity type having a top surface;

providing a first covering layer of semiconductor material of first conductivity type having a top surface and being contiguous to and overlying the substrate top surface;

providing a second covering layer of semiconductor material of second electrical conductivity type having

a top surface and being contiguous to the top surface of the first covering layer and extending vertically downward from the top surface of the first covering layer into an upper portion of the first covering layer;

providing a third covering layer of semiconductor material of heavily doped first conductivity type having a top surface and being contiguous to and partly overlying the top surface of the second covering layer, where a portion of the second covering layer is heavily doped and this portion extends vertically upward through the third covering layer to the top surface thereof and forms an exposed pattern of the second covering layer in the top surface of the third covering layer, and where the maximum depth of the heavily doped portion of the second covering layer relative to the top surface of the third covering layer is a predetermined number d_1;

providing a trench having side walls and bottom walls and extending vertically downward from the top surface of the third covering layer through the third and second covering layers and through a portion of, but not all of, the first covering layer, where the trench has a maximum depth relative to the top surface of the third covering layer equal to a second predetermined number d_2 and d_2 is less than d_1, where the trench in horizontal cross section is approximately a polygonal stripe, and where this polygonal stripe laterally surrounds and is spaced apart from the exposed pattern of the second covering layer at the top surface of the third covering layer;

providing a layer of oxide, positioned within the trench and contiguous to the bottom walls and side walls of the trench so that a portions of, but not all of, the trench is filled with this oxide layer;

providing electrically conducting semiconductor material, contiguous to the oxide layer and positioned within the trench so that the oxide layer lies between

the electrically conducting semiconductor material and the bottom and side walls of the trench; and

providing three electrodes that are electrically coupled to the electrically conducting semiconductor material in the trench, to the second covering layer and to the substrate, respectively.

15. The method according to Claim 14, further comprising the step of providing said trench with rounded corners of oxidized material, where said bottom surfaces and said side surfaces of said trench meet and where said side surfaces of said trench meet said top surface of said third covering layer and where said side surfaces of said trench meet with one another.

16. The method according to Claim 14, wherein said steps of providing said third covering layer and providing said trench include the step of choosing the difference d_1-d_2 of said first and second predetermined numbers d_1 and d_2 as 0.5 μm or greater.

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